



NAMAN GOYAL



ACADEMIC DETAILS

| Year | Degree / Board | Institute | GPA / Marks(%) |
|------|---|--------------------------------------|----------------|
| --- | B.Tech in Electrical Engineering (Power and Automation) | Indian Institute of Technology Delhi | 9.22 |
| 2024 | CBSE | M.M Public School | 92.6 |
| 2022 | CBSE | N.C Jindal Public School | 97.2 |

SCHOLASTIC ACHIEVEMENTS

- **Department Rank 1:** Among the students of Electrical Engineering (Power and Automation) from the past **2 semesters**.
- **International Physics Olympiad (IPhO): Gold Medalist** in INPhO and finished among top **37** students nationally.
- **International Astronomy Olympiad (IOAA): Gold Medalist** in INAO and finished among top **29** students nationally.
- **Informatics Olympiads:** Rank **1** in Croatian Open Competition in Informatics (COCI) | USA Computing Olympiad (USACO) **Gold**.
- **Math Olympiad:** Qualified Indian Qualifier in Mathematical Olympiad and invited to write test for national team selection for **IMO**.
- **Semester merit:** Awarded cash scholarship for being in **top 7%** students and Department Rank **1** for semester **1** and **3**.
- **Panini Linguistic Olympiad: Bronze Medalist** in Panini Linguistics Olympiad (**PLO**) Round 2, an olympiad in deductive reasoning.

INTERNSHIPS

- **CISPA Helmholtz Center for Information Security, Germany** | *Research Intern, Trusted Systems Group* (May 2026 - Jul. 2026)
 - Spearheaded a measurement study of **hardware supply-chain security** across **131 open-source RISC-V cpu and gpu cores**.
 - Forensically graded each core from **RTL, testbenches, and commit history** contrasting the results with their claims.
 - Architected the **13-dimensional, 50-attribute taxonomy** focusing on reproducibility, verification, and CI/CD resilience.
 - Built a reproducible Python data analysis pipeline yielding **40+** figures for the final measurement study presentation.
 - Uncovered **95%** repositories with no side-channel defenses, **77%** lacking secure boot; **co-authoring** a publication.

PROJECTS

- **QicQacQoe Quantum Game Simulator** | *Quantum Computing* | Prof. Rajendra Kumar (Mar. 2026)
 - Wrote a 13-qubit **quantum simulator** supporting configurable states and concurrent operations (Hadamard, CNOT, measurement).
 - Architected continuous **quantum state analysis** logic to calculate win conditions across superposition and entanglement.
- **Solovay–Kitaev Unitary Decomposer** | *Quantum Computing* | Prof. Rajendra Kumar (Feb. 2026)
 - Implemented the **Solovay–Kitaev algorithm** from scratch to **approximate** any **single-qubit gate** over a finite set.
 - Built a **precomputed** base-case **lookup table** with vectorized nearest-neighbor search and **group-commutator** decomposition.
- **Time-Travelling File System** | *Data Structures and Algorithms* | Prof. Rohit Vaish (Sep. 2025)
 - Engineered a Git-inspired **C++ version control system** utilizing custom-built **Heap** and **HashMap** data structures.
 - Architected a **pointer-based** memory management **framework** to enable robust file **snapshotting** and complete **history tracking**.
 - Implemented highly **efficient** state rollbacks and revision traversals, consistently achieving $O(\log n)$ branching complexity.
- **SocialNet** | *Data Structures and Algorithms* | Prof. Rajendra Kumar (Nov. 2025)
 - Engineered a **C++** social network backend utilizing custom-built **AVL Trees, Graph** data structures and algorithms.
 - Implemented **pointer-based** node management to seamlessly handle user interactions, post mapping, and network traversal.
- **KAN-PINN Battery SOH Model** | *Independent Project* (Jul. 2025)
 - Developed a **KAN-PINN** hybrid model to accurately predict battery state-of-health by embedding **physics-based constraints**.
 - Architected a custom training framework with **augmented Lagrangian methods** to enforce stability during optimization.
 - Built a scalable data processing pipeline to integrate physical battery metrics with high-fidelity neural network predictions.
- **4-bit Gray Code Counter** | *Digital Logic* | Prof. Manan Suri (Oct. 2025)
 - Designed a **4-bit Gray-Code** counter on Nexys Artix-7 **FPGA** using **Verilog**, ensuring minimal bit transitions across all states.
 - Optimized state logic using **Karnaugh maps** to optimise SR flip-flop input logic for efficient hardware resource usage.
- **Low-Latency C++ Execution Engine** | *Independent Project* (Jul. 2025)
 - Engineered a **low-latency trading pipeline** utilizing zero-allocation architectures and lock-free **SPSC ring buffers**.
 - Optimized throughput via **SIMD prefetching**, cache locality strategies, and strict compile-time polymorphism.
 - Architected a **multithreaded hardware-aware scheduler** utilizing CPU core pinning and precise memory orderings.

TECHNICAL SKILLS

- **Languages and Frameworks:** Python, C/C++, JavaScript, Verilog, React, Flask, Qiskit, MATLAB, TensorFlow, PyTorch
- **Tools and Libraries:** Vivado, Neovim, Docker, pandas, NumPy, Matplotlib, Scikit-learn, PyTorch, AutoDesk Inventor, Git

EXTRA CURRICULAR ACTIVITIES

- **Aries Research Executive:** Contributed to several technical and research projects at Aries, **IIT Delhi's AI society**.
- Academic Mentor for **MTL100** (calculus), guiding first-year students through single and multivariable calculus concepts.



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IIT COURSE

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COURSES DONE

Electromagnetic Waves & Qua.mec., Calculus, Data Structures And Algorithms, Signals And Systems, Digital Electronics, Circuit Theory, Calculus, Electromagnetic Waves & Qua.mec., Linear Algebra & Diffe. Equa., Professional Ethics And Social Responsibility - Ii, Quantum Computing, Probability & Stochastic Pro., Technology And Governance, Power Electr. & Energy Devices, Control Engineering I

EXTRA CURRICULAR ACTIVITIES

- Academic Mentor, Mentorship
- Research Team, ARIES